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SPECIFICATION

Phase Locked Loop (PLL) Circuit, Phase Synchronization Method and Operation Analysis Method for the Circuit

Technical Field

[0001]

The present invention relates to a Phase Locked Loop (PLL) circuit that produces a clock signal corresponding to a phase difference between a reference clock signal and a comparison clock signal, and also to a phase synchronization method for the circuit.

Background Art

[0002]

A patent document 1 (Unexamined Patent Publication No. 2004-40227) discloses a conventional PLL circuit, for example.

[0003]

The conventional PLL circuit is equipped with a phase comparator for comparing phase to produce an output signal having a phase difference proportional to a time difference between the duration of a rectangular wave signal having a high voltage level and that of a rectangular wave signal having a low voltage level. The duration of the rectangular wave signal having the high voltage level is equal to that of the rectangular wave

signal having the low voltage level when there is no phase difference. The conventional PLL circuit is configured so that the loop filter once required is omitted and a waveform shaping circuit for holding rectangular waveform of the output signal from the phase comparator is replaced for the loop filter omitted.

[0004]

A Voltage Controlled Oscillator (VCO) is designed on the assumption that the voltage-frequency variation characteristic of the VCO becomes an odd function when frequency variation is a function of voltage.

Patent Document 1: Unexamined Patent Publication No. 2004-40227

Disclosure of the Invention

Problems to be Solved by the Invention

[0005]

The thus configured conventional PLL circuit requires a VCO whose voltage-frequency characteristic becomes an odd function when the frequency variation is a function of voltage. On an actual VCO, such a characteristic exists only partially in the area, so that there is no choice but using such a limited area.

[0006]

Another problem is that a VCO is costly when such a characteristic exists in a large part of the area, which results in an increase in circuit costs.

[0007]

Another problem is that the phase comparator described in the

patent document 1, which is not a commonly used component, has to be specially designed, which accordingly pushes up the design costs.

[0008]

Still another problem is that the conventional PLL circuit uses the phase comparator, and accordingly an output frequency from the VCO varies even in a stationary mode when the phase is synchronized.

[0009]

An object of this invention is to attain a low cost PLL circuit that outputs a clock signal whose frequency varies little.

Means to Solve the Problems

[0010]

A phase locked loop (PLL) circuit according to this invention may be characterized by including:

a phase comparator that receives a reference clock signal and a comparison clock signal, compares a phase of the reference clock signal with a phase of the comparison clock signal, produces a rectangular wave signal having three voltage levels corresponding to phase differences, and outputs the rectangular wave signal;

a level shifter that receives the rectangular wave signal outputted from the phase comparator, shifts a voltage level of the rectangular wave signal, and outputs the rectangular wave signal whose voltage level has been shifted;

a voltage controlled oscillator (VCO) that receives the rectangular wave signal outputted from the level shifter, and outputs a clock signal

whose frequency corresponds to the voltage level of the rectangular wave signal; and

a frequency divider that divides the frequency of the clock signal outputted from the VCO by N (N is a counting number), and feeds back a signal whose frequency is divided to the phase comparator as the comparison clock signal.

[0011]

The phase comparator may be characterized by comparing the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal, and producing the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level.

[0012]

The phase comparator may be characterized by producing a rectangular wave signal having a high voltage level by making duration of the rectangular wave signal having the high voltage level proportional to a phase difference when the comparison clock signal has the phase difference caused by a phase lag, and producing a rectangular wave signal having a low voltage level by making duration of the rectangular wave signal having the low voltage level proportional to the phase difference when the comparison clock signal has the phase difference caused by a phase lead, and outputting a reference level signal without outputting the rectangular wave signal having the high or low voltage level when there is no phase difference.

[0013]

The level shifter may be characterized by converting three voltage levels, a voltage level of the rectangular wave signal having the high voltage level, a voltage level of the rectangular wave signal having the low voltage level, and a voltage level of the reference level, to a voltage level for controlling a VCO.

[0014]

The level shifter may be characterized by including a plurality of resistors connected in series; and a switch that produces the voltage level for controlling a VCO by switching connections of the plurality of resistors based on the three voltage levels.

[0015]

The phase comparator may be characterized by comparing the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal, and producing the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level.

[0016]

The VCO may be characterized by having an arbitrary voltage-frequency characteristic.

[0017]

The PLL circuit may be characterized in that a mathematical model is used as a principle of operation of the PLL circuit, the mathematical model expressing a response from the PLL circuit by a numeric sequence.

[0018]

A phase synchronization method for a phase locked loop (PLL)

circuit according to this invention may be characterized by including:

receiving a reference clock signal and a comparison clock signal, comparing a phase of the reference clock signal with a phase of the comparison clock signal, producing a rectangular wave signal having three voltage levels corresponding to phase differences, and outputting the rectangular wave signal;

receiving the rectangular wave signal, shifting a voltage level of the rectangular wave signal, and outputting the rectangular wave signal whose voltage level has been shifted;

receiving the rectangular wave signal whose voltage level has been shifted, and outputting a clock signal whose frequency corresponds to the voltage level of the rectangular wave signal; and

dividing a frequency of the clock signal by N (N is a counting number), and feeding back a signal whose frequency is divided to the phase comparator as the comparison clock signal.

[0019]

The phase synchronization method for a PLL circuit may be characterized by comparing the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal, and producing the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level.

[0020]

An operation analysis method for a phase locked loop (PLL) circuit according to this invention may be characterized by an operation analysis method for a PLL circuit including:

a phase comparator that receives a reference clock signal and a comparison clock signal, compares a phase of the reference clock signal with a phase of the comparison clock signal, produces a rectangular wave signal having a predetermined voltage level, duration of which corresponds to a phase difference, and outputs the rectangular wave signal;

a voltage controlled oscillator (VCO) that receives a signal outputted from the phase comparator, and outputs a clock signal whose frequency corresponds to a voltage level of the signal; and

a frequency divider that divides a frequency of a clock signal outputted from the VCO by N (N is a counting number), and feeds back a signal whose frequency is divided to the phase comparator as the comparison clock signal,

The operation analysis method may be characterized by including analyzing an operation for the phase difference between the reference clock signal and the compression clock signal by using a mathematical model expressed below:

$\theta_n=(1-((G\cdot T)/(2\pi\cdot N)))^n\cdot\theta$

n: a counting number

π: a circle ratio

G: a fixed number corresponding to the voltage-frequency characteristic of the VCO

T: an oscillation cycle of the reference clock signal

N: a frequency divisor (a counting number) of the frequency divider

θ: a phase difference at time 0

θ_n: a phase difference at time nT

Best Mode for Carrying out the Invention

[0021]

Embodiment 1.

A description is given below of a Phase Locked Loop (PLL) circuit 100 with reference to figures. A PLL circuit, also called a phase synchronization loop or the like, is a circuit to generate an output signal whose phase is not different from that of an input signal.

[0022]

In Fig. 1, an input terminal 1 is a terminal from which a reference clock signal FR is inputted.

[0023]

A phase comparator 2 compares the phases of incoming two signals, and outputs a phase difference detection signal PD corresponding to a phase difference between the signals. The phase comparator 2 outputs a rectangular wave signal having a high voltage (H) level and a rectangular wave signal having a low voltage (L) level. The phase comparator 2 outputs as the phase difference detection signal PD a rectangular wave corresponding to the phase difference and having duration of the H or L level rectangular wave signal proportional to the phase difference. The phase compactor 2 outputs reference level voltage when there is no phase difference.

[0024]

A level shifter 3 is a waveform-shaping device to hold rectangular waveform of the phase difference detection signal PD from the phase

comparator 2.

[0025]

A voltage controlled oscillator (VCO) 4, which has a control terminal, is an oscillator that can change oscillation frequency using the direct current voltage of a direct current signal DC applied to the control terminal. The VCO 4 is an oscillator to generate an oscillation clock signal CL that is N times the frequency of a reference clock signal (N is a counting number).

[0026]

A frequency divider 5 is a clock frequency divider to divide the frequency of the oscillation clock signal CL by N and output a comparison clock signal FP to the phase comparator 2.

[0027]

An output terminal 6 is a terminal that outputs the oscillation clock signal CL.

[0028]

Fig. 2 is a diagram illustrating an example of implementation of the level shifter 3.

[0029]

In Fig. 2, SW1 and SW2 denote analog switches to switch the contacts of signals based on the output level of a rectangular wave signal from the phase comparator 2. The SW1 is a switch that turns ON only when the phase difference detection signal PD is the H level rectangular wave signal. The SW2 is a switch that turns ON only when the phase difference detection signal PD is the L level rectangular wave signal. In

other situations, both the SW1 and the SW2 are OFF. The SW1 and the SW2 never turn ON at the same time.

[0030]

R1, R2, R3 and R4 denote resisters (or resistance values thereof) to set out the voltage level of the direct current signal DC to be inputted to the VCO 4. The R1, the R2, the R3 and the R4 are connected in series and to which a voltage Vcc is applied.

[0031]

The following shows the switching conditions of the SW1 and the SW2 depending on the output level of the rectangular wave signal from the phase comparator 2. The voltage level at that time of the direct current DC to be inputted to the VCO 4 is described below.

[0032]

When the SW1 is ON and the SW2 is OFF, then

Voltage Level =Vcc×((R3+R4)/(R1+R3+R4))

with a high voltage level because the R2 is bypassed. A signal having this high voltage level (or the voltage level thereof) will be referred to hereinafter as V_H.

[0033]

When the SW1 is OFF and the SW2 is ON, then

Voltage Level =Vcc×((R4)/(R1+R2+R4))

with a low voltage level because the R3 is bypassed. A signal with this low voltage level (or the voltage level thereof) will be referred to hereinafter as V_L.

[0034]

When the SW1 is OFF and the SW2 is OFF, then

Voltage Level =Vcc×((R3+R4)/(R1+R2+R3+R4))

with a reference voltage between V_H and V_L because the R1 through the R4 are all connected. A signal with this reference voltage (or the voltage level thereof) will be referred to hereinafter as V_n ($V_H>V_n>V_L$).

[0035]

Fig. 3 is a diagram illustrating the voltage-frequency characteristic of the VCO 4.

[0036]

In Fig. 3, the horizontal axis shows the input voltage v of the direct current signal DC to the VCO 4. The input voltage v ranges from 0V to Vcc V.

[0037]

The vertical axis shows an output frequency f of the oscillation clock signal CL from the VCO 4. A frequency f_0 is assumed to be 1/N of a frequency fr of the reference clock signal FR. When the input voltage v is 0V, then the output frequency f becomes a frequency f_0-df. When the input voltage v is Vcc V, then the output frequency f does not however become a frequency f_0+df. When the V_H and the V_L are appropriately chosen, then the following may be obtained.

[0038]

The V_n is the reference voltage whose output frequency f becomes the frequency f_0.

[0039]

The V_L is the low voltage whose output frequency f becomes a

frequency f_0-Δf.

[0040]

The V_H is the high voltage whose output frequency f becomes a frequency f_0+Δf.

[0041]

A relation among the three voltage levels is $V_H > V_n > V_L$. It is not always true, however, that $V_H - V_n = V_n - V_L$.

[0042]

Referring to Fig. 3, it is apparent from the graph showing a characteristic that frequency variation from the frequency f_0 of the output frequency f becomes:

$g(V_H) = -g(V_L) = \Delta f$, $g(V_n) = 0$

when it is the function g(v) of the input voltage v.

[0043]

That is, $\Delta f = G$ (G is a fixed number).

[0044]

Level setting is made in advance so that the level shifter 3 generates voltages such as V_H, V_n, and V_L. More specifically, the level shifter 3 set the levels so that a difference (Δf) between an output frequency to the VCO corresponding to an H level output and a clock frequency of a reference voltage and a difference ($-\Delta f$) between an output frequency to the VCO corresponding to an L level output and the clock frequency of the reference voltage are equal in absolute value but different in sign.

[0045]

With regard to frequency, the oscillation clock signal CL in a

steady state may be expressed as:

$f_0=N\times fr, fr=fp$

where f_0 denotes the frequency of the oscillation clock signal CL, fr denotes the frequency of the reference clock signal FR, and fp denotes the frequency of the comparison clock signal FP.

[0046]

Fig. 4 is a diagram showing the concept of a basic operation of the phase comparator 2 and the level shifter 3.

[0047]

The horizontal axis shows time. The vertical direction shows a signal waveform of the reference clock signal FR, a signal waveform of the comparison clock signal FP, an output waveform of the phase difference detection signal PD from the phase comparator 2, and the voltage of the direct current signal DC from the level shifter 3 or the input voltage v to the VCO 4.

[0048]

Fig. 4 shows the case of a phase difference of θ between the comparison clock signal FP and the reference clock signal FR. The phase comparator 2 detects this phase difference θ. A phase lag of the comparison clock signal FP is denoted by $-\theta$ and a phase lead of the comparison clock signal FP is denoted by $+\theta$.

[0049]

The phase comparator 2, when detecting a phase lag, outputs the rectangular wave signal having the voltage Vcc during a period from time t1 to time t2 to advance the phase (in order to turn the SW1 ON). The

level shifter 3, upon receipt of the rectangular wave signal having the voltage Vcc, turns the SW1 ON, so that the voltage is changed to V_H, to output the direct current signal DC. Operations like this are repeated in series until the n-th cycle (n is a counting number) where a phase difference θ_n (n is a counting number) is processed, which attains a synchronous phase finally at time t3 of the n-th cycle (Fig. 4 shows a case of n=1).

[0050]

The phase comparator 2 outputs a signal having a voltage Vcc/2 with a synchronous phase. The level shifter 3, upon receipt of a signal having the voltage Vcc/2, turns the SW1 and the SW2 both OFF, so that the voltage is changed to V_n, to output the direct current signal DC. Alternatively, the level shifter 3 keeps the SW1 and SW2 OFF, and outputs the direct current signal DC whose voltage is kept to a voltage V_n.

[0051]

The phase comparator 2, when detecting a phase lead, outputs the rectangular wave signal having a voltage 0 (GND) during a period from time t4 to time t5 to delay the phase (in order to turn the SW2 ON). The level shifter 3, upon receipt of the rectangular wave signal having the voltage 0, turns the SW2 ON, so that the voltage is changed to V_L, to output the direct current signal DC. Operations like this are repeated in series until the n-th cycle (n is a counting number) where the phase difference θ_n (n is a counting number) is processed, which attains a synchronous phase finally at time t6 of the n-th cycle (Fig. 4 shows a case of n=1).

[0052]

Fig. 5 is a diagram illustrating the waveform of a detection signal having a phase difference of θ between the comparison clock signal FP and the reference clock signal FR when detected by the phase comparator 2.

[0053]

Referring to Fig. 5, the horizontal axis shows time. The vertical direction shows the voltage of the current signal DC, that is, the voltage level of the input voltage v to the VCO 4.

[0054]

T (T=1/fr) denotes duration of one cycle of the reference clock signal FR.

[0055]

V_n denotes reference voltage for reference. The V_n is the same as that shown in Fig. 3 and Fig. 4.

[0056]

V_L is low voltage corresponding to an L level portion. The V_L is the same as that shown in Fig. 3 and Fig. 4. The V_L is a signal for delaying the phase.

[0057]

V_H is high voltage corresponding to an H level portion. The V_H is the same as that shown in Fig. 3 and Fig. 4. The V_H is a signal for advancing the phase.

[0058]

The V_H is convex and the V_L is concave in shape.

[0059]

In Fig. 5, the V_H rises at the middle of a cycle (half the cycle time or T/2) and holds the high voltage during a period of $(\theta/2\pi)T$ and then returns to the reference voltage.

[0060]

The V_L holds the low voltage during a period of $(\theta/2\pi)T$ before the middle of the cycle (T/2) and then returns to the reference voltage at the middle of the cycle (T/2).

[0061]

With reference to Fig. 4, the V_H and the V_L are outputted to the same positions as where there are phase differences, respectively. Like the case of Fig. 5, however, when the phase comparator 2 outputs the phase difference detection signal PD with T/2 as a core, then the V_H and the V_L are outputted after and before T/2, respectively. The phase may thus be adjusted within one cycle T without fail.

[0062]

Duration between the V_H and the V_L is equivalent to the period of $(\theta/2\pi)T$. In other words, the duration between the V_H and the V_L is proportional to the phase difference θ. For this reason, the frequency becomes $f_0+\Delta f$ or $f_0-\Delta f$ of the oscillation clock signal CL during the period of $(\theta/2\pi)T$. Consequently, the phase of the oscillation clock signal CL is advanced or delayed by an amount proportional to θ.

[0063]

A description is now given of a phase synchronization method for the PLL circuit 100 with reference to an operational flowchart of Fig. 6.

[0064]

Inputting Step S1

Initially, the reference clock signal FR inputted through the input terminal 1 for the reference clock signal is inputted to the phase comparator 2. The oscillation clock signal CL from the VCO 4 is divided by N in the frequency divider 5, and then inputted to the phase comparator 2 as the comparison clock signal FP.

[0065]

Phase Comparing Step S2

Next, with the phase comparator 2, the phase of an incoming reference clock signal FR is compared with the phase of an incoming comparison clock signal FP. The phase comparator 2 then outputs, according to a phase difference, a rectangular wave of the H or L level rectangular wave signal whose duration is proportional to the phase difference as the phase difference detection signal PD.

[0066]

The phase comparator 2, when detecting a phase lag of the comparison clock signal FP, outputs the H level rectangular wave signal having Vcc V to turn the SW1 ON in order to advance the phase. The duration of the H level rectangular wave signal is proportional to the phase difference. The period of duration is equivalent to the period of $(\theta/2\pi)T$.

[0067]

The phase comparator 2 outputs a signal having Vcc/2 V when there is no phase difference.

[0068]

The phase comparator 2, when detecting a phase lead of the

comparison clock signal FP, outputs the L level rectangular wave signal having 0V (GND) to turn the SW2 ON in order to delay the phase. The duration of the L level rectangular wave signal is proportional to the phase difference. The period of the duration is equivalent to the period of $(\theta/2\pi)T$.

[0069]

Now, the output of the phase comparator 2 is assumed as follows.

[0070]

The H level is almost equivalent to the power supply voltage of Vcc, which is sufficiently higher than Vcc/2 in electric potential. The L level is almost equivalent to a ground potential GND=0V, which is sufficiently lower than Vcc/2 in electric potential.

[0071]

The standard level is almost equivalent to Vcc/2, which is sufficiently lower than Vcc but sufficiently higher than GND in electric potential.

[0072]

This setting may be achieved by selecting the values of the R1, the R2, the R3, and the R4 (e.g., R1, R4<R2, R3).

[0073]

Level Shifting Step S3

The phase difference detection signal PD outputted from the phase comparator 2 is inputted to the level shifter 3.

[0074]

Now, the level shifter 3 is configured as shown in Fig. 2, for

example. The SW1 of Fig. 2 is now assumed to operate on receiving an almost Vcc in electric potential and short the R2, but not to operate on receiving any other values in electric potential. The SW2 of Fig. 2 is also assumed to operate on receiving an almost GND in electric potential and short the R3, but not to operate on receiving any other values in electric potential.

[0075]

The level shifter 3 eliminates overshoot or undershoot from the phase difference detection signal PD, converts the H level to:

$V_H=Vcc\times((R3+R4)/(R1+R3+R4))$,

the L level to:

$V_L=R4/(R1+R2+R4)$,

the reference level to:

$V_n=(R3+R4)/(R1+R2+R3+R4)$,

and inputs a result to the VCO 4 as a frequency controlled voltage for the VCO 4.

[0076]

Oscillation Step S4

The VCO 4 converts the duration of the H level rectangular wave signal to an amount of phase to be eliminated during the period of one cycle, and then oscillates. The VCO 4 also converts the duration of the L level rectangular wave signal to an amount of phase to be added during the period of one cycle, and then oscillates.

[0077]

More specifically, frequency controlled voltages to be inputted to the

VCO 4 of one cycle T include the amount of phases to be added or eliminated during the one cycle as the duration of the H or L level rectangular wave signal. The VCO 4 reads this duration and oscillates the oscillation clock signal CL whose phase has been controlled according to the duration.

[0078]

Fig. 4 shows the operation described above. When the phase of the comparison clock signal FP lags behind the phase of the reference clock signal FR, then the level shifter 3 outputs the V_H during duration proportional to the corresponding phase difference. When the phase of the comparison clock signal FP leads the phase of the reference clock signal FR, the level shifter 3 then outputs the V_L during duration proportional to the corresponding phase difference. When neither the V_H nor the V_L is outputted, then the level shifter 3 keeps outputting the V_n.

[0079]

When there is no phase difference between the comparison clock signal FP and the reference clock signal FR, or good phase synchronization is achieved, then the V_n is also outputted.

[0080]

Outputting Step S5

The oscillation clock signal CL outputted from the VCO 4 diverges into a signal to be outputted to outside via the output terminal 7 as an output from the PLL circuit and a signal inputted to the frequency divider 5.

[0081]

Frequency-dividing Step S6

The oscillation clock signal CL is divided by N in the frequency divider 5, and then fed back to the phase comparator 2 as the comparison clock signal FP.

[0082]

According to the PLL circuit of this embodiment, an output from the phase comparator 2 becomes the stationary reference level voltage of Vcc/2 after the phase is synchronized, and an output from the level shifter receiving this voltage also becomes the stationary reference level of V_n of the VCO 4. It may be expected therefore that an output frequency from the VCO 4 or an output frequency from the PLL circuit is a clock output with little variation.

[0083]

With this embodiment, the PLL operation is not described by a transfer function, but treated as a numeric sequence of an adjustment amount of phase of one cycle of the reference clock signal FR. Fig. 5 shows a waveform of the detection signal when the phase comparator 2 detects a phase lag or lead of θ between the comparison clock signal FP and the reference clock signal FR, for example.

[0084]

With reference to the H level portion and the L level portion of this waveform when V_n is a reference line, the H level portion is a phase lead element and the L level portion is a phase lag element as shown in Fig. 5 based on the characteristics of the VCO 4 of Fig. 3.

[0085]

More specifically, when a phase lag of θ of the comparison clock signal FP behind the phase of the reference clock signal FR is detected, then the phase of the comparison clock signal FP may be advanced by an amount proportional to the phase difference θ between the reference clock signal FR and the comparison clock signal FP by the phase lead element shown in Fig. 5. When a phase lead of θ of the comparison clock signal FP ahead of the phase of the reference clock signal FR is detected, then the phase of the comparison clock signal FP may be delayed by an amount proportional to the phase difference θ between the reference clock signal FR and the comparison clock signal FP by the phase lag element shown in Fig. 5.

[0086]

Thus, the PLL circuit according to this embodiment is equipped with the phase comparator 2 that compares the phase to produce an output signal having three-level outputs of the H level rectangular wave signal, the L level rectangular wave signal, and the reference level, and outputs the H or L level signal having duration corresponding to a detected phase difference or outputs a standard level voltage when there is no phase difference detected.

[0087]

The PLL circuit according to this embodiment is also equipped with the level shifter 3 that serves to hold rectangular waveform of the output signal from the phase comparator 2.

[0088]

The level shifter 3 is to set the levels of the output voltages (V_n, V_H,

V_L) so that the difference (Δf) between the output frequency ($f_0+\Delta f$) of the VCO 4 corresponding to the H level output V_H and the clock frequency (f_0) of the reference voltage V_n and the difference (Δf) between the output frequency ($f_0-\Delta f$) of the VCO 4 corresponding to the L level output V_L of the level shifter 3 and the clock frequency (f_0) of the reference voltage V_n are equal in absolute value but different in sign ($|\Delta f|=|-\Delta f|$).

[0089]

The PLL circuit according to this embodiment is to perform operation analysis and designing by the numeric sequence where the phase difference of one cycle of the reference clock signal is a unit of measurement. This is explained as follows.

[0090]

An explanation is now given for a mathematical model that describes these circuit operations quantitatively.

[0091]

When a phase difference between the reference clock signal FR and the comparison clock signal FP is θ at time t=0, then a phase difference $\psi(t)$ at time t>0 is given by the following expression.

[0092][Expression 1]

$$\psi(t) = \theta - \frac{1}{N} \cdot \int_0^t g(v(x))dx$$

[0093]

When θ_{n-1} is a phase difference between the reference clock signal FR and the comparison clock signal FP (a result of the phase of the reference clock signal FR minus the phase of the comparison clock signal

FP) at time t=(n-1)T(n=1,2,3,···), the voltage v(t) to be inputted to the VCO 4 during the period of (n-1)T<t<nT is given below. When a step function U(t):

[0094][Expression 2]

$$U(t)=\begin{cases}1, & t>0\\ 0, & t<0\end{cases}$$

[0095]

is used, and

[0096][Expression 3]

$$\tau_n=(n-1)T+\frac{|\theta_{n-1}|}{2\pi}T$$

[0097]

is defined, then the following expression is given when the phase of the comparison clock signal FP lags behind the phase of the reference clock signal FR ($\theta_{n-1}>0$).

[0098][Expression 4]

$$v(t)=V_H\cdot U[t-(n-1)T]-V_H\cdot U(t-\tau_n)$$
$$+V_n\cdot U(t-\tau_n)-V_n\cdot U(t-nT)$$

[0099]

This expression is the same as the following expression:

[0100][Expression 5]

$$v(t)=\begin{cases}V_H, & (n-1)T<t\le\tau_n\\ V_n, & \tau_n<t\le nT\end{cases}$$

[0101]

in value.

[0102]

When the v(t) is plugged into g(v), and g is converted to the function of time t, then the following expression is obtained.

[0103][Expression 6]

$$g(t)=\begin{cases} g(V_H)=\Delta f=G, & (n-1)T<t\le\tau_n \\ g(V_n)=0, & \tau_n<t\le nT \end{cases}$$

[0104]

Likewise, when the phase of the comparison clock signal FP leads the phase of the reference clock signal FR ($\theta_{n-1}<0$), then the following expression is obtained.

[0105][Expression 7]

$$v(t)=V_L\cdot U[t-(n-1)T]-V_L\cdot U(t-\tau_n)$$
$$+V_n\cdot U(t-\tau_n)-V_n\cdot U(t-nT)$$

[0106]

This expression is the same as the following expression:

[0107][Expression 8]

$$v(t)=\begin{cases} V_L, & (n-1)T<t\le\tau_n \\ V_n, & \tau_n<t\le nT \end{cases}$$

[0108]

in value.

[0109]

When the v(t) is plugged into g(v), and g is converted to the function of time t, then the following expression is obtained.

[0110][Expression 9]

$$g(t)=\begin{cases} g(V_L)=-\Delta f=-G, & (n-1)T<t\le\tau_n \\ g(V_n)=0, & \tau_n<t\le nT \end{cases}$$

[0111]

Therefore, the amount of frequency variation g(t) when $(n-1)T<t\leqq nT$ is given by the following expression including ($\theta_{n-1}>0$) and ($\theta_{n-1}<0$) together.

[0112][Expression 10]

$$g(t)=\frac{\theta_{n-1}}{|\theta_{n-1}|}\cdot G\cdot\{U(t-(n-1)T)-U(t-\tau_n)\}$$

[0113]

The phase difference θ_n when t=nT may be calculated by using this expression.

[0114][Expression 11]

$\theta_n=\psi(nT)$

$$\begin{aligned} &= \theta-\frac{\theta_{n-1}}{|\theta_{n-1}|}\cdot\frac{G}{N}\cdot \\ &\quad\left[\sum_{k=1}^{n-1}\int_{(k-1)\cdot T}^{k\cdot T}\left[U\left(t-(k-1)\cdot T\right)-U\left(t-\tau_k\right)\right]dt\right] \\ &\quad-\frac{\theta_{n-1}}{|\theta_{n-1}|}\cdot\frac{G}{N}\cdot \\ &\quad\int_{(n-1)\cdot T}^{n\cdot T}\left[U\left(t-(n-1)\cdot T\right)-U\left(t-\tau_n\right)\right]dt \\ &= \theta_{n-1}-\frac{\theta_{n-1}}{|\theta_{n-1}|}\frac{G}{N}\cdot \\ &\quad\int_{(n-1)\cdot T}^{n\cdot T}\left[U\left(t-(n-1)\cdot T\right)-U\left(t-\tau_n\right)\right]dt \end{aligned}$$

[0115]

The definite integration of this expression may be calculated as

follows:

[0116][Expression 12]

$$\theta_n = \left(1 - \frac{G \cdot T}{2\pi \cdot N}\right) \cdot \theta_{n-1}$$

[0117]

which is a recurrence formula that expresses a geometric sequence.

[0118]

Therefore, the following expression is the mathematic model of the phase difference variation of each cycle T.

[0119][Expression 13]

$$\theta_n = \left(1 - \frac{G \cdot T}{2\pi \cdot N}\right)^n \cdot \theta$$

[0120]

The convergence condition of this sequence should be a lockup condition of the PLL circuit of this embodiment. In addition to this, the following expression:

[0121][Expression 14]

$$0 < \frac{G \cdot T}{\pi \cdot N} < 4$$

[0122]

should be satisfied.

[0123]

This means, in other words, the PLL circuit will surely be locked up regardless of the value of the initial phase difference θ (when time t=0) as long as the above condition is satisfied.

[0124]

This also shows that the phase difference becomes 0 in the period of one cycle when $GT/N\pi=2$.

[0125]

More specifically, the use of the mathematical model of this embodiment may provide a method of analyzing the operation of the PLL circuit, and at the same time, show a response operation of the PLL circuit of this embodiment to a step phase input. This also makes it possible to design the lockup time.

[0126]

Thus, the PLL circuit according to this embodiment is characterized by having the phase comparator that compares the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal. The phase comparator outputs the rectangular wave signal having three levels of the high voltage level, the low voltage level, and the reference level. The duration of the rectangular wave signal having the high or low voltage level is proportional to the phase difference. The phase comparator does not output the rectangular wave signal having the high or low voltage level when there is no phase difference, but outputs the reference level.

[0127]

The PLL circuit is also characterized by having the voltage-controlled oscillator (VCO) that outputs the clock signal having a frequency corresponding to the level of a voltage level applied. The PLL circuit is also characterized by feeding back the signal obtained by dividing

the clock signal outputted from the VCO by N (N is a counting number) to the phase comparator as the comparison clock signal.

[0128]

The PLL circuit is further characterized by having the level shifter that converts the voltage levels of the rectangular wave signal having the high voltage level, the rectangular wave signal having the low voltage level, and the reference level, which are outputted from the phase comparator, to the controlled voltage level as an appropriate input to the VCO.

[0129]

The PLL circuit may thus be provided with the VCO having an arbitrary voltage-frequency characteristic.

[0130]

In addition to this, the PLL circuit uses the mathematical model that describes the response of the PLL circuit by numeric sequence as the operation principle.

Industrial Applicability

[0131]

As described above, the PLL circuit according to this embodiment, the phase comparator having the three-level outputs is a type called a "phase-frequency comparator" and commonly in an integrated circuit (IC). The use of such a general phase comparator may eliminate the need for designing a special comparator, so that the PLL circuit may be obtained with a reduction in design costs.

[0132]

Once the phase is synchronized, only the stationary reference level voltages are inputted to the VCO, so that the output frequency from the PLL circuit has little variation.

[0133]

When the phase convergence condition, i.e.,

[0134][Expression 15]

$$|\theta_n| < \varepsilon$$

(where ε is a maximum value of an acceptable phase difference when the phase is synchronized)

[0135]

is determined, then the convergence speed is computable directly by n that satisfies this phase convergence condition. An advantageous feature of a conventional PLL circuit of n×T is maintained.

[0136]

Further, with the convergence conditional expression of numeric sequence, the convergence area is twice that of the conventional PLL circuit, so that the PLL circuit with greater flexibility in circuit design may be obtained.

Brief Description of the Drawings

[0137]

[Fig. 1] It is a block diagram of a PLL circuit to explain a first embodiment of the present invention.

[Fig. 2] It is a block diagram illustrating an example of implementation of a level shifter used in the first embodiment of the present invention.

[Fig. 3] It is a diagram illustrating a voltage - frequency characteristic of a

VCO used in the PLL circuit according to the first embodiment of the present invention.

[Fig. 4] It is a diagram illustrating a concept of the basic operations of a phase comparator and the level shifter used in the first embodiment of the present invention.

[Fig. 5] It is a diagram to explain a mathematical model of the PLL circuit according to the first embodiment of the present invention.

[Fig. 6] It is a diagram illustrating a phase controlling method of the PLL circuit according to the first embodiment of the present invention.